IN THE CLAIMS:

Please amend claims 1 and 10; withdraw claims 13-15; delete claims 19 and 20 and add new claim 21 as follows:

1. (Currently Amended) A high electron mobility transistor using a Group III-V compound semiconductor, comprising :

an undoped second channel layer laminated on an InP substrate via a buffer layer;

an undoped first channel layer laminated on said second channel layer; and

a doped electron-supplying layer laminated on said first channel layer,

wherein said first channel layer is composed of $In_{1-x}Ga_xAs$ and has an energy ~~layer~~ level of conduction band lower than that of said electron-supplying layer,

said second channel layer is composed of a Group III-V compound semiconductor using a Group V element other than P, has an energy level of conduction band higher than that of the first channel layer, has a band gap wider than that of the first channel layer, and has a thickness larger than that of the first channel layer.

2. (Original) The high electron mobility transistor as described in claim 1, wherein said first and second channel layers are formed to have a thickness small enough to have discrete quantum levels, a first quantum level being formed only in the first channel layer, and a second quantum level being formed in both the first and second channel layers.

3. (Previously Amended) The high electron mobility transistor as described in claim 1, wherein said electron-supplying layer is composed of $In_{1-y}Al_yAs$, the first channel layer is composed of $In_{1-x}Ga_xAs$, and the second channel layer is composed of $In_{1-x}(Al_{1-z}Ga_z)_xAs$.

4. withdrawn

5. (Previously amended) The high electron mobility transistor as described in claim 3, wherein the thickness of said first channel layer is 3~7 nm.

6. (Previously amended) The high electron mobility transistor as described in claim 3, wherein the thickness of said second channel layer is 10~20 nm.

7. (Previously amended) The high electron mobility transistor as described in claim 3, wherein the composition ratio (1-z) of Al element in said second channel layer is 0.05~0.5.

8. (Previously Amended) The high electron mobility transistor as described in claim 1, wherein said electron-supplying layer is composed of $In_{1-y}Al_yAs$, the first channel layer is composed of $In_{1-x}Ga_xAs$, and the second channel layer is composed of $In_{1-x}Ga_xAs$ with the In composition ratio lower and the gallium composition ratio higher than those in the first channel layer.

9. (Previously Amended) The high electron mobility transistor as described in claim 1, wherein an element separation groove is formed which extends from said electron-supplying layer to said buffer layer.

10. (Currently Amended) A high electron mobility transistor using a Group III-V compound semiconductor, comprising :

an undoped second channel layer laminated on an InP substrate via a buffer layer and composed of $In_{1-x}(Al_{1-z}Ga_z)_xAs$ (where the composition ratio (z-1) of Al is 0.05~0.5) which is lattice matched to InP,

an undoped first channel layer laminated on said second channel layer and composed of $In_{1-x}Ga_xAs$ which is lattice matched to InP, and

a doped electron-supplying layer laminated on said first channel layer and composed of $In_{1-y}Al_yAs$ which is lattice matched to InP.

11. (Original) The high electron mobility transistor as described in claim 10, wherein said first and second channel layers are formed to have a thickness small enough to have the discrete quantum levels, a first quantum level being formed only in the first channel layer, and a second quantum level being formed in both the first and second channel layers.

12. (Currently Amended) A high electron mobility transistor using a Group III-V compound

semiconductor, comprising

an undoped second channel layer laminated on an InP substrate via a buffer layer;

an undoped first channel layer laminated on said second channel layer; and

a doped electron-supplying layer laminated on said first channel layer,

wherein said first channel layer is composed of $In_{1-x}Ga_xAs$ and has an energy ~~layer~~ level of conduction band lower than that of said electron-supplying layer,

said second channel layer is composed of a Group III-V compound semiconductor using a Group V element other than P, has an energy level of conduction band higher than that of the first channel layer, and has a band gap wider than that of the first channel layer,

wherein said electron-supplying layer is composed of $In_{1-y}Al_yAs$, the first channel layer is composed of $In_{1-x}Ga_xAs$, and the second channel layer is composed of $In_{1-x}(Al_{1-z}Ga_z)_xAs$,

wherein the composition ratio (1-z) of Al element in said second channel layer is 0.05~0.5.

13. withdrawn

14. withdrawn

15. withdrawn

16. (Previously Added) The high electron mobility transistor as described in claim 2, wherein said electron-supplying layer is composed of $In_{1-y}Al_yAs$, the first channel layer is composed of $In_{1-x}Ga_xAs$, and the second channel layer is composed of $In_{1-x}Ga_xAs$ with the In composition ratio lower and the gallium composition ratio higher than those in the first channel layer.

17. (Previously Added) The high electron mobility transistor as described in claim 2, wherein an element separation groove is formed which extends from said electron-supplying layer to said buffer layer.

18. (Previously Added) The high electron mobility transistor as described in claim 2, wherein said electron-supplying layer is composed of $In_{1-y}Al_yAs$, the first channel layer is composed of $In_{1-x}Ga_xAs$, and the second channel layer is composed of $In_{1-x}(Al_{1-z}Ga_z)_xAs$.

19. Deleted

20. Deleted

21. (New) A high electron mobility transistor using a Group III-V compound semiconductor, comprising:

an undoped second channel layer laminated on an InP substrate via a buffer layer;

an undoped first channel layer laminated on said second channel layer; and

a doped electron-supplying layer laminated on said first channel layer,

wherein said first channel layer is composed of $In_{1-x}Ga_xAs$ and has an energy ~~layer~~ level of conduction band lower than that of said electron-supplying layer,

said second channel layer is composed of a Group III-V compound semiconductor using a Group V element other than P, has an energy level of conduction band higher than that of the first

channel layer, has a band gap wider than that of the first channel layer, and has a thickness larger than that of the first channel layer

wherein the doped electron-supplying layer, the undoped first channel layer and the undoped second channel layer are the group III-V compound semiconductor being lattice-matched to the InP substrate.